Claim Amendments:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for fabricating sidewall spacers in the manufacture of an integrated circuit device, comprising:

providing a substrate having a gate structure formed thereon;

forming a dielectric spacer layer over the semiconductor substrate; and

etching said dielectric spacer layer without the use of a sacrificial forming spacer to form L-shaped spacers for the gate structure, the L-shaped spacers including a first L-shaped spacer adjacent to a first sidewall of the gate structure and a second L-shaped spacer adjacent to a second sidewall of the gate structure, wherein a horizontal portion of the L-shaped spacer varies gradually to provide for an average thickness of the L-shaped portion that is 50 to 85 percent of the maximum thickness.

2. (Previously Presented) The method of Claim 1, further including forming a liner oxide layer over said gate structure prior to forming the dielectric spacer layer.

3. (Previously Presented) The method of Claim 2 wherein said liner oxide layer is deposited to a thickness of between approximately 20 Angstroms and 200 Angstroms.

4. (Previously Presented) The method of Claim 1 wherein said dielectric spacer layer comprises a nitride layer.

5. (Previously Presented) The method of Claim 3, wherein the said dielectric spacer has a thickness in the range of 150 Angstroms and 500 Angstroms.

6. (Previously Presented) The method of Claim 1 wherein said dielectric spacer layer comprises a silicon oxynitride layer.

7. (Previously Amended) The method of Claim 1 wherein etching said dielectric spacer layer includes anisotropically etching said dielectric spacer layer to form L-shaped spacers, said L-shaped spacers having vertical portions varying in thickness and horizontal portions varying in thickness.

8. (Currently Amended) The method of Claim 7, wherein said horizontal portion of the L-shaped spacers having bulging profiles varying gradually in thickness from a maximum thickness immediately adjacent the vertical portion of the L-shaped spacer to a portion of the L-shaped spacer furthest from the vertical-portion of the L-shaped spacer~~, wherein the horizontal portion varies gradually to provide for an average thickness of the L-shaped portion that is 50 to 85 percent of the maximum thickness~~.

9. (Previously Presented) The method of Claim 7 wherein said dielectric spacer layer is anisotropically etched using a capacitively coupled plasma etch process with an etching chemistry comprising CH3F and O2 in combination with an inert gas to form said L-shaped spacers.

10. (Previously Presented) The method of Claim 7, wherein said dielectric spacer layer is anisotropically etched using an inductively coupled plasma etch process with an etching chemistry comprising CH3F and O2 in combination with an inert gas.

11. (Previously Presented) The method of Claim 1, wherein etching said dielectric spacer layer to form said L-shaped spacers includes using CH3F and O2 chemistry in ratios ranging from approximately 2:1 to approximately 5:1 CH3F to O2.

12. (Previously Presented) The method of Claim 11, wherein etching said dielectric spacer layer to form said L-shaped spacers utilizes a pressure during the etch process ranging from approximately 20 milliTorr to approximately 500 milliTorr.

13. (Previously Presented) The method of Claim 11, wherein etching includes using a temperature ranging from approximately 10 degrees C and 30 degrees C.

14. - 17. (Canceled)

18. (Previously Presented) A method for fabricating sidewall spacers in the manufacture of an integrated circuit device, comprising:

providing a substrate having a gate structure formed thereon;

forming a liner oxide layer on said gate structure;

forming a dielectric spacer layer over said liner oxide layer; and

anisotropically etching said dielectric spacer layer without the use of a sacrificial forming layer to form L-shaped spacers, said L-shaped spacers having vertical portions and a horizontal portion, wherein the horizontal portion varies gradually in thickness from a maximum thickness immediately adjacent the vertical portion of the L-shaped spacer to a portion of the L-shaped spacer furthest from the vertical-portion of the L-shaped spacer, wherein the horizontal portion varies gradually to provide for an average thickness of the L-shaped portion that is 50 to 85 percent of the maximum thickness.

19. (Previously Presented) A method for fabricating sidewall spacers in the manufacture of an integrated circuit device, comprising:

providing a substrate having a gate structure formed thereon;

forming a dielectric spacer layer over the semiconductor substrate having a first exposed surface portion adjacent to a first sidewall of the gate structure and a second exposed surface portion adjacent to a second sidewall of the gate structure; and

etching said first and second exposed surface portions of the dielectric spacer layer while forming first and second L-shaped spacers for the gate structure at respective locations of the first and second exposed surface portions.

20. (Previously Presented) The method of Claim 19, further including forming a liner oxide layer over said gate structure prior to forming the dielectric spacer layer.

21. (Previously Presented) The method of Claim 20 wherein said liner oxide layer is deposited to a thickness of between approximately 20 Angstroms and 200 Angstroms.

22. (Previously Presented) The method of Claim 19 wherein said dielectric spacer layer comprises a nitride layer.

23. (Previously Presented) The method of Claim 21, wherein the said dielectric spacer layer has a thickness in the range of 150 Angstroms and 500 Angstroms.

24. (Previously Presented) The method of Claim 19 wherein said dielectric spacer layer comprises a silicon oxynitride layer.

25. (Previously Presented) The method of Claim 19 wherein etching said dielectric spacer layer includes anisotropically etching said dielectric spacer layer to form L-shaped spacers, said L-shaped spacers having vertical portions varying in thickness and horizontal portions varying in thickness.

26. (Previously Presented) The method of Claim 25, wherein said and horizontal portion of the L-shaped spacers having bulging profiles varying gradually in thickness from a maximum thickness immediately adjacent the vertical portion of the L-shaped spacer to a portion of the L-shaped spacer furthers from the vertical-portion of the L-shaped spacer, wherein the horizontal portion varies gradually to provide for an average thickness of the L-shaped portion that is 50 to 85 percent of the maximum thickness.

27. (Previously Presented) The method of Claim 25 wherein said dielectric spacer layer is anisotropically etched using a capacitively coupled plasma etch process with an etching chemistry comprising CH3F and O2 in combination with an inert gas to form said L-shaped spacers.

28. (Previously Presented) The method of Claim 25, wherein said dielectric spacer layer is anisotropically etched using an inductively coupled plasma etch process with an etching chemistry comprising CH3F and O2 in combination with an inert gas.

29. (Previously Presented) The method of Claim 19, wherein etching said dielectric spacer layer to form said L-shaped spacers includes using CH3F and O2 chemistry in ratios ranging from approximately 2:1 to approximately 5:1 CH3F to O2.

30. (Previously Presented) The method of Claim 29, wherein etching said dielectric spacer layer to form said L-shaped spacers utilizes a pressure during the etch process ranging from approximately 20 milliTorr to approximately 500 milliTorr.

31. (Previously Presented) The method of Claim 29, wherein etching includes using a temperature ranging from approximately 10 degrees C and 30 degrees C.

32. (Currently Amended) A method for fabricating sidewall spacers in the manufacture of an integrated circuit device, comprising:

providing a substrate having a gate structure formed thereon;

forming a dielectric spacer layer over the semiconductor substrate; and

etching said dielectric spacer layer, prior to forming any layer overlying the dielectric spacer layer, to form L-shaped spacers from the dielectric spacer layer for the gate structure, the L-shaped spacers including a first L-shaped spacer adjacent to a first sidewall of the gate structure and a second L-shaped spacer adjacent to a second sidewall of the gate structure.

33. (Previously Presented) A method for fabricating sidewall spacers in the manufacture of an integrated circuit device, comprising:

forming a dielectric spacer layer overlying a gate structure formed on a substrate; and

etching said dielectric spacer layer without the use of a sacrificial forming spacer to form L-shaped spacers, wherein etching said dielectric spacer layer includes anisotropically etching said dielectric spacer layer to form L-shaped spacers, said L-shaped spacers having vertical portions varying in thickness and horizontal portions varying in thickness, the horizontal portions having bulging profiles varying gradually in thickness from a maximum thickness immediately adjacent the vertical portion of the L-shaped spacer to a portion of the L-shaped spacer furthest from the vertical-portion of the L-shaped spacer, wherein the horizontal portion varies gradually to provide for an average thickness of the L-shaped portion that is 50 to 85 percent of the maximum thickness.